An Improved Performance of Minimum Cost Spanning Application for VLSI Interconnects

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Abstract-Elmore delay is extensively used model in both digital circuit interconnects design and analog that recent to compute signal delays. General Elmore delay models was used in the studies of various process in delay technologies [1]. Besides the Elmore delay model, different delay model presented in the literature that contain inductive effects in order to increase accuracy (an analytic delay). The person that was applied this model to RC circuit is Rubinstein et al in 1983[2]. The classical Elmore delay general form is defined then solve by applying the indicated boundary. The input signal effect of the rise is considered in [3]. The classical Elmore and the new improvement of Elmore delay was compared by using SPICE simulation that the result varies the accuracy of delay formation. The result shows that an improved delay interconnection provided a better precision.

Keywords: VLSI Interconnects, Elmore Delay

I. INTRODUCTION

The Elmore delay is still used in various application such as in the different metric definitions (as delay matric). Whether it was in thick or high, now the interconnection delay donate up to 50-70% of clock cycle [4] and becoming major concern in the high speed of system design. At this state, the development of classical layout design objective such as chip area no longer enough because different consideration is required on system performance. The minimum Steiner tree has been chosen as interconnect topology because it results in a minimum wire capacitance as it is used minimum wiring area which is the major factor in conventional technology of interconnect delay. But the minimum delay is no longer achieved by minimum Streiner tree in the design of high speed interconnects [5].

A smaller delay result in the latter tree. The first problem necessarily to be address is performance analysis in order to study performance-driven interconnect design. The relationship between interconnect structure and interconnection delay are normally very slow and fails to reveal even though the circuit performance can be run by numerical simulator such as SPICE.

The constant reduction of the feature size has been dynamic force behind the VLSI rapid growth of technology. The size decreased from about 2µm in 1985, to 1µm in 1990 and to 0.5-0.35 µm in 1996 and 0.18 in 2001[6]. The strong impact towards VLSI technology as the continuous miniaturization of VLSI in few ways. First of all, the features size is decreased quadratically on circuit of the device density. The total number of transistors has increased from less 500 000 in 1985 to over 10 million on single VLSI today as a result. Next, the interconnect delay becomes more significant at a high rate. Based on simple scaling rule explain in [6], the factor S reduce the intrinsic delay by a where the local interconnects remain the same when the devices are scale down in all three dimensions by a factor S but factor S^2 increased the delay of world-wide interconnects. The interconnect delay become the dominating factor in determining system performances as the result. There an about 50-70% of clock cycle are consumed by interconnect delay in system designed today.

The variable that determined the interconnect delay such as interconnect resistance, gate resistance and loading capacitance. The driver resistance is a minimum cases that was used in the interconnect resistance that trivial in lump loading capacitor also known as interconnect and loading gate [7]. The driver resistance times with the total loading capacities in order to estimate internet delay. Then, by using the buffer insertion and minimum length, the driver resistance using driver, gate, transistor sizing, minimum-width routing also the minimizing the interconnect capacitance are focused to reduce in conventional technique. As the deep submicron technology are now become available, indirectly the

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driver resistance is comparable to the interconnect resistance [8]. The optimal buffer placement, optimal wire sizing simultaneous driver has become necessary and important technique.

II. BACKGROUND

The few steps involved in VLSI design included high level design, physical layout not to forget is logic design. Basically, the number of functional block or also known as cells that are interconnect, is usually in design. A set of bits $\{S_0, S_1, S_2,...,S_k\}$ are a net *k* composed which must electrically connected. A S₀ supplies a signal to interconnect which symbolizes the driver of the set. A net may have multiple drivers in some cases that each driving the interconnect at a different time. In a net sink that consist a set of wire, the remaining bits collect the signal from the driver which often represented by a graph. The edge vertex symbolizes a bit or a combine of two wire segment and signify a wire segment.

High-performance interconnect topology optimization

The first thing to optimize the high-performance interconnection is to list all the topology for maintenance interconnect. Then, consider the major design goals for this problem which consist the total interconnect length of wire and the path of length/diver to connected one server timing-critical sink if minimization. The wire length minimization contains several advantages such as the total capacitance still donates a wire length minimization is interest for a reason such as the total wire capacitance still denotes a significant even the wire resistance are considered [9].

Total wirelength minimization topology optimization

The interconnect optimization is effected by contributor problem caused from the minimization of the wire. The problems in VLSI interconnect design is directly applicable based on research using the construction of minimum spanning tress (MST) and Steiner minimal trees (SMT). To avoid ambiguity with the abbreviation MST, the abbreviation SMT for Steiner trees is used.

Minimum spanning trees

The issue involving MST is to find a set of edges T that connect a given point M with the minimal total cost. There are two traditional algorithms to solve this problem [7]. The Kruskal's algorithm [10] which start with trees forest (singleton vertices) in current forest

iterative which join two trees, then two value of the lower cost are adds until all M point remain connected by a single tree. The Prim's algorithms [11] begin with adding an connected vertex by an arbitrary node that act as the roof of partial tree then using the less cost edge till no unconnected vertex exist.

III. METHODOLOGY

The Elmore delay offers a simple form expression with significantly improved accuracy for delay measure compared to the lumped RC circuit that act as main advantage and even the applicability is inadequate to the step function type of input signal but it easily integrated into design and computerization. A very large scale very large-scale integration (VLSI) interconnects result show that Elmore delay analysis both tree cost and tree radius on signal delay on connection distributed RC tree structures.

The input to output of the input signal delay are explained in the Elmore delay model. The 0.5 percent point delay of the monotonic step response time. Then the step response of RC circuit is h(t) are express in the following equation:

$$\int_{0}^{t_{p}} h(t)dt = 0.5$$
 (1)

The formula to calculate the Elmore delay for RC interconnect can be expressed as follow:

$$T_{p}\sum_{i=1}^{n}R_{ik}C_{i}$$
(2)

Where *N* is total number of nodes in RC corresponding, R_{ik} is the resistance of the portion of the path to the C_i where stand for capacitance at node *i*. then the impulse response of Laplace transform is

$$H(s) = \int_{0}^{\infty} h(t) e^{-st} dt$$
(3)

After e^{-st} is expanded about s = 0, the expression function can be expressed as

$$m_{i} = \frac{1}{i!} (-1)^{i} \int_{0}^{\infty} h(t) t^{i} dt$$
(4)

The circle of the Elmore delay is form when is the first order moment. Elmore delay can be calculated to

be more accurate if the moment that are taken into account is higher. Besides that, the upper bound can be created into the boundaries while arbitrary input was accounted the median of the impulse response. The mean and median are equivalent whereas the function input was used in the Elmore delay.

The more accurate delay calculations can be formed at the expense of computational effort if the higher order moments are taken into account. In the Elmore delay formulation, the median of the impulse response accounts for the arbitrary input waveform, while the mean of the impulse response created an upper bound for the delay. The mean and medium are equal whereas the Elmore delay is used in step function inputs. Figure 1 shows the VLSI interconnect model and its lumped RC are equivalent.



Figure 1. (a) A VLSI interconnect with n=1(lumped model), (b) RC equivalent circuit [12]

Compound interest problem

This method was discovered by Jacob Bernoulli and the compound interest problem was investigate. This can be formulated as follow:

$$\lim_{n \to \infty} \left(1 + \frac{1}{n}\right)^n$$
(5)

Euler's number is main by the continuous Bernoulli trials for a specific experiment. The continuous Bernoulli trials for a detailed experiment also lead to Euler's number.

Improved delay model

Based on Figure 2, the unit length L = 1 is assumed and limitation G define shown as below

$$G = \frac{1}{\tau} \tag{6}$$

$$\tau = RC$$
 (7)

where the τ is conductor of total delay time. Then G = 1. Then in Figure 3, the conductor detached into two part.



Figure 2. (a) A VLSI interconnect with n=2(lumped model), (b) RC equivalent circuit [12]

The traditional Elmore delay design has the same computational cost when compared to the improved Elmore delay.

IV. RESULT

In order to compare the traditional and improved Elmore delay, the SPICE simulations for a distinctive VLSI interconnect are compared. The same partnership calculation to estimate the Elmore delay and improved model formulation variant the delay with n from SPICE as shown in Figure 3. Based on the result shown in Figure 4, the traditional and improved Elmore delay percentage error that respect to SPICE simulation [12]. The outcomes shown that improved delay gives a better accuracy in the final

consequences.



Figure 3. Variation of the delay of typical interconnect simulated with SPICE and calculated by the traditional and improved Elmore delay models against n [12]



Figure 4. The percentage of errors for the classical and improved delay formation with respect to SPICE simulations [12]

V. CONCLUSION

In conclusion, the presented formulation has improved Elmore delay. The advancement of the new model is considered as the premise for the lower bound of the formulation. There exists the curve fitting used by the delay model in the literature. It proved that it gives the better accuracy even though the traditional Elmore model and improved takes the equal computational difficulty. Formulations for applying the probability distribution function approach are investigated. SPICE simulations are performed to confirm the precision of model that a new proposed in typical VLSI interconnect. The improved Elmore delay gives a lot of advantage such as easily integrated in automation design without any computational cost increment.

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